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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/726,474

12/01/2003

Masood Murtuza

TI-35639

5891

23494 7590 02/09/2007
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EXAMINER

DICKEY, THOMAS L

ART UNIT

PAPER NUMBER

2826

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

02/09/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/726,474

Applicant(s)

MURTUZA, MASOOD

Examiner

Thomas L. Dickey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5,7,8,10,12-14 and 24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5,7,8,10,12-14 and 24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/28/06 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 1-5, 7,8, 10, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by DAVIS ET AL. (2003/0197280).

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With regard to claims 1-5, 7,8, and 10, Davis et al. discloses a semiconductor device comprising a substrate 51; a plurality of inter-level dielectric (ILD) layers 61-65-69 each having a low dielectric constant (k) (note paragraph 0033) and at least one (being made from SiLK™, note paragraph 0037) having an ultra low dielectric constant (k); at least one support structure (via) 47 formed from a copper support material and disposed in each of the ILD layers 61-65-69 at locations overlying each other so that support structures 47 overly each other in the plurality of layers to mitigate damage of the semiconductor device caused by stresses to the ILD layers 61-65-69; at least one additional ILD layer 73 having a dielectric constant which (being made from silicon oxide or silicon nitride) is higher than the low-k ILD layers 61-65-69 overlying the low-k inter-level dielectric layers, the support column ending at the at least one additional ILD layer 73; and a contact layer 37-38 overlying the at least one additional ILD layer 73 and the support structures 47, wherein the at least one additional ILD layer 73 isolates the contact layer 37-38 from the support structures 47. Note figures 4 and 5 and paragraphs 0029-0036 of Davis et al.

With regard to claim 24, Davis et al. discloses a semiconductor device comprising a substrate 51; a plurality of inter-level dielectric (ILD) layers 61-65-69 each having a low dielectric constant (k) (note paragraph 0033); at least one support structure 47 disposed in each of the ILD layers 61-65-69 at locations overlying each other so that support structures 47 overly each other in the plurality of layers to mitigate damage of the semiconductor device caused by stresses to the ILD layers 61-65-69; at least one additional ILD layer 73 having a

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dielectric constant which (being made from silicon oxide or silicon nitride) is higher than the low-k ILD layers 61-65-69 overlying the low-k inter-level dielectric layers; and a bond pad 45 overlying the at least one additional ILD layer 73 and the support structures 47. Note figures 4 and 5 and paragraphs 0029-0036 of Davis et al.

The applicant's claims 1,5,7,8, and 24 do not distinguish over the Davis et al. reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of mitigating damage of the semiconductor device caused by stresses to the ILD layers, mitigating damage following application of stress from a bond pad; and mitigating damage of the IILD layer due to forces applied onto the ILD layer during one of a subsequent processing and packaging of the semiconductor device.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. See *In re Ludtke and Sloan*, 169 USPQ 563 at 567, and *In re Swinehart* 169 USPQ 226, both of which make it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also *In re Schreiber*, 44 USPQ2d 1429, 1432 (Fed. Cir. 1997), for a discussion of the roles of examiner and

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applicant in determining when and how functional limitations distinguish a claim from prior art disclosing the same structure.

B. Claims 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by TSAU (2002/0038903).

Tsau discloses a semiconductor device comprising a substrate 102; a plurality of inter-level dielectric (ILD) layers 108, 116, 146, 156, 166 each having a low dielectric constant (k); and a least one support structure 128, 138, 148, 158, 168 disposed in each of the ILD layers 108, 116, 146, 156, 166 at locations overlying each other so that support structures 128, 138, 148, 158, 168 overlie each other in the plurality of layers 108, 116, 146, 156, 166; at least one additional ILD layer 169 having a dielectric constant which is higher than the low-k ILD layers 108, 116, 146, 156, 166 overlying the low-k inter-level dielectric layers; and a contact layer M5 (including contacts 170 and 175, note paragraph 0079) overlying the at least one additional ILD layer 169 and the support structures 128, 138, 148, 158, 168; wherein a plurality of support structures 128, 138, 148, 158, 168 are disposed in the at least one of the low-k dielectric layers in an $n \times m$ matrix (note figures 5c, 5e, 5g, and 5i) configuration, where n and m are integers greater than one, wherein a plurality of support structures 128, 138, 148, 158, 168 are disposed in the at least one low-k dielectric layer at a plurality of locations spaced equidistant apart from each other across substantially the entire layer, and the plurality of support structures 128, 138, 148, 158, 168 are disposed at a location below a bond pad location 170 disposed on the semiconductor device.

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The applicant's claims 12 and 13 do not distinguish over the Tsau reference regardless of the functions allegedly performed by the claimed device, because only the device per se is relevant, not the recited functions of mitigating damage of the semiconductor device caused by stresses to the ILD layers 108,116,146,156,166 and mitigating damage of the ILD layer due to forces applied onto the ILD layer during one of a subsequent processing and packaging of the semiconductor device.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. See *In re Ludtke and Sloan*, 169 USPQ 563 at 567, and *In re Swinehart* 169 USPQ 226, both of which make it clear that it is the patentability of the device per se which must be determined in a "functional language" claim and not the patentability of the function, and that an old or obvious device alleged to perform a new function is not patentable as a device, whether claimed in "functional language" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also *In re Schreiber*, 44 USPQ2d 1429, 1432 (Fed. Cir. 1997), for a discussion of the roles of examiner and applicant in determining when and how functional limitations distinguish a claim from prior art disclosing the same structure.

Response to Arguments

3. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

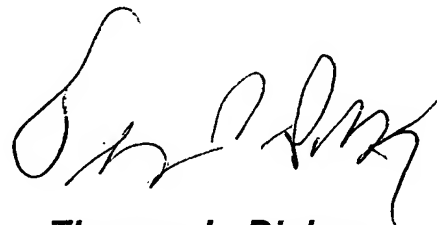
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Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**Thomas L. Dickey
Primary Examiner
Art Unit 2826**